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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,730	12/10/2003	Rui M. Bastos	NVDA P000573	6695
26291	7590	04/26/2005	EXAMINER	
MOSER, PATTERSON & SHERIDAN L.L.P. 595 SHREWSBURY AVE, STE 100 FIRST FLOOR SHREWSBURY, NJ 07702			TUNG, KEE M	
			ART UNIT	PAPER NUMBER
			2676	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/732,730

Applicant(s)

BASTOS ET AL.

Examiner

Kee M Tung

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 17-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

1. Claims 17-20 has been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 3/2/05. A complete reply to this Office action must include cancellation of nonelected drawn claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (6,118,452).

Gannett teaches a graphics processor (Fig. 1A, 116) configured to produce data for multiple output buffers (col. 8, lines 61-67, respective buffers in the frame buffer 232), each output buffer associated with a unique output buffer identifier (not explicitly teach or suggest by Gannett, however, Gannett teaches "drawn into an **appropriate** frame buffer" (col. 8, lines 4-7); and "respective **buffers** in the frame buffer 232, include a color buffer, depth buffer, accumulation buffer and stencil buffer" (col. 8, lines 61-67). It would have been obvious to one of ordinary skill in the art at the time the present invention was made that a buffer identifier would have been obvious in order for each of the fragment operation stages to store or identifier their respective buffer in more

efficient and effective manner and thus to improve the system performance.), comprising a fragment processing pipeline (168) configured to process graphics data to produce processed graphics data for the multiple output buffers and determine at least one output buffer identifier associated with the processed graphics data; a shader read interface (frame buffer controller in side the frame buffer and control 170) configured to read processed graphics data associated with an output buffer identifier from an output buffer stored in a memory; and a write interface (also by the frame buffer controller which controls both read from and write to the frame buffer) configured to write processed graphics data associated with at least one output identifier to an output buffer stored in the memory. Therefore, at least claims 1 and 9 would have been obvious.

As per claim 2, Gannett fails to explicitly suggest or teach a geometry processor configured to process graphics data. However, as well known in the graphics art, a graphics subsystem (or processor or controller) includes a front end processor which is called geometry processor and a back end subsystem (or processor or controller) is called rasterizer or renderer. Therefore, the teaching of geometry processor is an inherent in view of the teachings of graphics processor of Gannett.

As per claim 3, Gannett teaches at least one output buffer identifier is determined by a fragment program executed in the fragment processing pipeline (such as, the one of the fragment modules in Fig. 20).

As per claim 4, Gannett teaches an output buffer includes data represented in two or more data formats (such as, different formats for pixel color for color buffer and depth value for Z-buffer).

As per claim 5, Gannett teaches the output buffer identifier is readable and writable by the fragment processing pipeline (enable each fragment operation stage to store their respective data into its buffer).

As per claim 6, Gannett teaches any of the multiple output buffers is selected for display (abstract).

As per claim 7, Gannett fails to explicitly teach or suggest the fragment processing pipeline includes multiple registers, each register capable of outputting data to one or more of the multiple output buffers. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of fragment operation stages of Gannett because a register (or a buffer) is a temporary storage device for storing data between components in order to overcome idle time when the next stage is not ready to accept the data.

As per claim 8, Gannett teaches the fragment processing pipeline determines an address associated with the processed fragment data, the address corresponding to a specific location in an output buffer (obvious by the teachings of "drawn into an appropriate frame buffer" (col. 8, lines 4-7) and "respective buffer" (col. 8, line 64)).

Claims 10 and 11 are similar in scope to claim 1, and thus are rejected under similar rationale.

As per claim 12, Gannett teaches the processed fragment data stored in the output buffer includes fragment depth data (col. 8, lines 65 and 66).

As per claim 13, Gannett teaches the processed fragment data stored in the output buffer includes an index (see clear value block box inside 170 includes a **clear index**).

As per claim 14, Gannett fails to explicitly teach or suggest the index is a shader identifier. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Gannett as claimed because the function of any index is used for easily identifying any identity, such as, a processor. Therefore, claim 14 would have been obvious by the teachings of index clear of Gannett.

As per claim 15, Gannett fails to explicitly teach or suggest the index is a pointer to a fragment program. It would have been obvious to one of ordinary skill in the art at the time the present invention was made that the feature would have been obvious in view of the teachings of well known and well used OpenGL specification in the computer graphics art.

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (6,118,452) as applied to claims 10 and 13 above, and further in view of Mori et al (6,704,018 hereinafter "Mori").

The teachings of Gannett are given in previous paragraph of this Office action. However, Gannett fails to explicitly teach or suggest the processed fragment data stored in the output buffer includes displaced mesh data. This is what Mori teaches (Fig. 9). Mori further teaches a computer graphics system (Fig. 1) comprising a graphics processor (Fig. 2, 8) includes vertex processor (30), a cache (70), a frame

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memory access unit (50), rendering processor (40), and a frame memory (80). The frame memory (Fig. 3) further includes multiple buffers (801-806). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Mori into the system of Gannett in order to draw high quality 3D compute graphics in real time as taught by Mori (col. 1, lines 13-15). Therefore, at least claim 16 would have been obvious.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Kee M Tung
Primary Examiner
Art Unit 2676